Form 1449*

Atty. Docket No.: 303.678US3

Serial No. Unknown

INFORMATION DISCLOSURE STATEMENT
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Applicant: Kie Y. Ahn et al.

Filing Date: Herewith

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U.S. PATENT DOCUMENTS

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**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
20	_ 5,668,035	09/16/1997	Fang, C.H., et al.	438	239	06/10/96	
	_ 5,985,725	11/16/1999	Chou, J.	438	294	12/23/97	
	_ 6,087,225	07/11/2000	Bronner, G.B., et al.	438	275	02/05/98	
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- 37	_ 6,222,788	04/01/2001	Forbes, et al.	365	230.06		

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PP	Chen, Y., et al., "Performance and Reliability Assessment of Dual-Gate CMOS Devices with Gate Oxide Grown Nitrogen Implanted Si Substrates", <u>International Electron Device Meeting</u> . pg. 1-4, (1997)
Po	Cho, I.H., et al., "Highly Reliable Dual Gate Oxide Fabrication by Reducing Wet Etching Time and Re-Oxidation for Sub-Quarter Micron CMOS Devices", Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, pgs. 174-175, (1999)
r b	Crowder, S., et al., "Trade-offs in the Integration of High Performance Devices with Trench Capacitor DRAM", Dig. Int. Electron Devices Meeting, Washington, D.C., pp. 45-48, (Dec. 1997)
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Sheet 2 of 2

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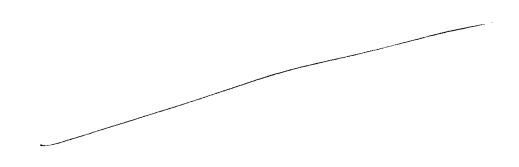
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PD	King, Y., et al., "Sub-5nm Multiple-Thickness Gate Oxide Technology Using Oxygen Implantation", <u>IEDM Technical Digest</u> , pp. 585-588, (1998)
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